CUSTOMER NO.: 24498
Serial No.: 10/518,226
Office Action dated: October 5, 2005

PATENT
PU020288

REMARKS

The Office Action mailed October 5, 2005 has been reviewed and carefully considered. It is respectfully asserted that no new matter has been added.

Claims 1, 2, 12, 14, 15, and 20 have been amended. Claims 1-23 are pending.

Claims 1-11, 14-17, and 20-23 stand rejected under 35 U.S.C. §112, second paragraph.

Claim 1 has been amended to now recite, *inter alia*, "identifying, from said parity check for each one of said N rows of said data block, from said parity check for each one of said X columns of said data block and from said at least one identified bad bytes for said data block, at least one error in said data block". Accordingly, the specified phrase of Claim 1 is now believed to be clear and not confusing.

Claim 2 has been amended to now recite, *inter alia*, "wherein said at least one bad byte for said data block is identified using at least one of an 8B/10B encoding process and an 8B/10B decoding process".

Claims 14 and 20 have been amended to now recite, *inter alia*, "wherein said confirmed error bits are identified using a combination of information derived from 8B/10B encoding of said data block, information derived from parity encoding along each row of said data block and information derived from parity encoding along each column of said data block"

Claims 15 and 21 have been amended to now recite, *inter alia*, "wherein identifying at least one suspect bit of said data block further comprises identifying at least one bad byte of said data block using information derived from said 8B/10B encoding of said data block".

Accordingly, all of the pending claims are now believed to satisfy 35 U.S.C. §112, second paragraph. Reconsideration of the rejection is respectfully requested.

Claims 1-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,559,506 to Leitch.

Claims 1 and 12 have been amended to further clarify and illustrate the invention. Support for the preceding amendments may be found at least at page 10, lines 3-11 of the Applicant's specification.

It is respectfully asserted that Leitch does not teach or suggest "performing a parity check for each one of said X columns of said data block, the parity check for each of said N rows and said X columns for detecting bit-level errors; identifying at least one bad byte for said data block using a byte-level error detection process", as now recited in amended Claim 1.

It is respectfully asserted that Leitch does not teach or suggest "wherein said identifying step identifies the at least one suspect bit using information derived from a byte-level error detection process and information derived from a bit-level error detection process", as now recited in amended Claim 12.

While the Examiner has admitted that "Leitch does not explicitly teach the identifying at least one bad byte for the data block" (Office Action, p. 4), the Examiner has nonetheless asserted that the preceding limitations are obvious. The Applicant respectfully disagrees.

The Examiner's reasoning, as reproduced from page 4 of the pending Office Action, is as follows:

Leitch teaches (figure 18) that within each tier (steps 1810, 1880, 1890), the (Q+S) symbols in each of the (Q+S) columns is checked for parity errors (1830). The symbol corrector (940) determines all possible error patterns which satisfy the row and column parity checking results and identifies which of the possible errors are non-ambiguous or ambiguous and corrects such errors therefrom (steps 1840-1870) (column 18 line 59-column 19 line 26).

It would have been obvious to one skilled in the art at the time the invention was made to realize that such checking row and column parity errors for each tier would encompass for checking errors for each tier itself. One have ordinary skill in the art would be motivated to do so because Leitch teaches that each tier of the N tiers would expand to (Q=S) columns and (R+T) rows by encoding the tier (figure 5, column 9, lines 35-58).

However, the preceding approach by Leitch nonetheless employs a **row-level error detection** (see, e.g., Leitch, col. 15, lines 8-19; see also, Leitch, FIG. 3, element 425, row parity encoder, and FIG. 12, element 910 row parity checker) and **column-level error detection** process (see, e.g., Leitch, col. 15, lines 27-38; see also, Leitch, FIG. 3, element 426, row parity encoder, and FIG. 13, element 930 row parity checker), that proceeds by tier (with each tier expanded to Q+S columns by the row parity encoder by adding S parity bits to each row and to R+T rows by the column parity encoder by adding T column parity bits, see, e.g., Leitch, col. 9, lines 28-44), where

each tier is "QxR information symbols includ[ing] R rows having Q information symbols in each row, and includ[ing] Q columns having R information symbols in each column" (Leitch, col. 2, lines 31-34).

As explicitly disclosed in Leitch, "[t]he parity checking results alone cannot always determine which of the data symbols need to be corrected" (Leitch, col. 15, lines 49-50). Accordingly, Leitch further discloses, at column 15, line 51 to column 16, line 16:

> The symbol corrector 940 identifies errors determined by the row parity checker 910 (FIG. 12) and column parity checker (FIG. 13) as ambiguous errors or non-ambiguous errors. Non-ambiguous errors ... are corrected when they are identified. Ambiguous errors are resolved in two ways. The symbol corrector 940 (FIG. 13) uses a quality value decoding technique in which the symbol corrector 940 evaluates a tier of data symbols to correct those which have ambiguous errors. ... The symbol corrector 940 (FIG. 13) also uses a burst assumption technique when ambiguous errors remain, in which row and column parity equations are used to identify all possible remaining data symbols having ambiguous errors, and the ambiguous errors are removed by selecting a set of the possible data symbols which are related best by having been sequentially transmitted (i.e., the best burst pattern is selected), upon an assumption that burst errors are probable.

In contrast, as noted above, Claim 1 recites performing parity checks for bit-level error detection and identifying at least one bad byte using a byte-level error detection process, while Claim 12 recites identifying at least one suspect bit using information derived from a byte-level error detection process and from a bit-level error detection process. Such an approach overcomes the prior art limitations of encoding/decoding processes that simply detect errors on a byte-level basis such as, e.g., 8B/10B encoding/decoding (see, e.g., Applicant's specification, p. 2, lines 8-11).

The Applicant respectfully asserts that a row or column does not correspond to a bit or a byte. A byte includes 8 bits. There is no such restriction on the number of bits a row or column in Leitch may include. As data is often "processed" in bytes, the present invention is particularly suited for programs and data structures that operate using bytes.

Accordingly, Leitch does not teach or suggest all of the limitations of independent Claims 1 and 12.

"To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art" (MPEP §2143.03, citing *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)).

Thus, Claims 1 and 12 are patentably distinct and non-obvious over the cited references for at least the reasons set forth above.

"If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious" (MPEP §2143.03, citing *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)).

Claims 2-11 depend from Claim 1 or a claim which itself is dependent from Claim 1 and, thus, includes all the elements of Claim 1. Claims 13-23 depend from Claim 12 or a claim which itself is dependent from Claim 12 and, thus, includes all the elements of Claim 12. Accordingly, Claims 2-11 and 13-23 are patentably distinct and non-obvious over the cited reference for at least the reasons set forth above with respect to Claims 1 and 12, respectively.

In view of the foregoing, Applicants respectfully request that the rejection of the claims set forth in the Office Action of October 5, 2005 be withdrawn, that pending claims 1-23 be allowed, and that the case proceed to early issuance of Letters Patent in due course.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to applicant's Deposit Account No. 07-0832.

Respectfully submitted,
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12/29/05 Linda Tindall

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